REMARKS

Claims 1-44 were previously pending in this application, with claims 4, 29 and 30 having been amended in the response to the last Office Action. With this response, claims 1, 26 and 34 are amended. No new claims are added. No claims are cancelled. As a result claims 1-44 are pending for examination.

Allowable Subject Matter

Claims 7, 9-11, 18 and 22 are indicated to contain allowable subject matter. At this time, Applicant defers a rewriting of these claims to independent form, in light of this request for reconsideration.

Drawings

The Applicant is pleased to note that the Examiner has withdrawn the objection to the drawings and that the drawings as filed with the Amendment of July 24, 2006 are acceptable.

Claim Rejections - 35 USC 103

Claims 1, 12-14, 26 and 31-33 have been rejected under 35 USC 103(a) as being unpatentable over Lee et al - U.S. Patent No. 6,329,863 in view of Bradley et al - U.S. Patent No. 6,550,664.

The rejection is flawed. In forming this rejection, the Examiner appears to have misapprehended or at least mis-characterized Lee, and mistaken the scope of claim 1. Despite the Examiner's assertions to the contrary, Lee does not describe "**[a]n** integrated circuit", which is the subject matter of claim 1. The semiconductor device 1 shown in Figure 1 of Lee is not an integrated circuit. To the contrary, it is a packaged device comprising a **plurality** of integrated circuits, not a **single** integrated circuit (i.e., one die) as is claimed in both original and amended claim 1. Lee clearly teaches a plurality of integrated circuits, provided on a plurality of dies. For example, Figures 1 and 2 of Lee show two dies (100 and 200) which are enclosed in separate packages (190 and 290) in Figure 3. In essence, Lee appears to be of the type of device known

in the art as a packaged device comprising a plurality of integrated circuits, such as a system-in-a-package (SIP) or a multi-chip module (MCM). The present invention, in contrast, is a single integrated circuit - just one die. While it is believed that the wording "An integrated circuit" was sufficient to differentiate from the disclosure of Lee, the amendment offered herein, where it is detailed that the invention is directed to an "integrated circuit comprising, on a single die...", should redundantly clarify how the presently claimed invention is structurally different from that of Lee.

With due respect to the Examiner's assertions to the contrary, it is evident that *an integrated circuit provided on a single die* is different from *a packaged device having a plurality of integrated circuits provided on a plurality of dies* as in Lee. This difference is not a trivial one and is directly related to the purpose of each disclosure. Lee teaches a packaged structure which is *well-suited for a stacked chip configuration (abstract)*. In the description of each and every figure in Lee wherever multiple paths are provided, they are not multiple paths within the same integrated circuit, but between integrated circuits.

Examples of the use of such multiple integrated circuits that are accessed through the same pin are discussed as being, for example, the provision of redundant memory, which was discussed in our previous response. The present invention, by contrast, teaches the provision of multiple signal paths within the same integrated circuit to increase the functionality of that individual integrated circuit. Multiple signal paths within a single integrated circuit is not the same as multiple integrated circuits each having an individual signal path at an "external" connection (i.e., a connection to another die in the package, not to the outside").

Thus, the Examiner's assertion that the present invention differs from Lee solely in the provision of a pad cell including a first signal path and a second signal path is flawed. From the first three words of Claim 1- **An integrated circuit**- the claim is different from the teaching of Lee. Claim 1 is directed to an article of manufacture and the words "an integrated circuit" are thus not part of a preamble that might deserve no patentable weight. The rest of the claim has to be read in the context that all of the subsequently mentioned features are provided as part of that single integrated circuit. There is no teaching in Lee recognizable to the person of ordinary skill in the art as suggesting, or even applicable to, the type of article defined in the presently claimed

invention. Therefore, even if one were to combine Lee's teachings with that of Bradley, one would not arrive at the claimed invention since neither document relates to "an" integrated circuit having the recited features on a single die.

Moreover, (1) Bradley does not suggest a migration of a multi-path arrangement to exterior connections and (2) the Examiner's assessment of Bradley appears to be flawed as well.

It is not merely a designer's choice as to where to locate the features of claim 1, as between a single die or a multiple die arrangement. Incorporation of the features of claim 1 into a single die permits the manufacture of an integrated circuit having a desirable feature exposed to the exterior pins whereas Lee only shows a feature internal to the multi-chip assembly. There is thus a qualitative difference, not merely a difference in degree.

The Examiner appears to believe (using the wording of the Office Action) that Bradley *teaches a pad cell (Fig. 4, 12)...* and includes *a first signal path (Fig. 4, 19) and a second signal path (Fig. 4, 20).* However the element corresponding to reference numeral 12 of Bradley is not a pad cell at all; rather, it is the die. In this regard, the Examiner's attention is directed to the description related to Figure 4, specifically paragraph [0018].

> *[0018] FIG. 4 shows a film bulk acoustic resonator (FBAR) filter* ***die 12*** *mounted in a microwave package using flip chip bonding technology in accordance with a preferred embodiment of the present invention. FBAR filter* ***die 12*** *includes a film bulk acoustic resonator filter circuit such as that shown in FIG. 1.* ***Bonding pads of FBAR filter die 12 are attached via solder joints to signal paths*** *within a bottom layer 18 of a ceramic package 10. This is illustrated in FIG. 4* ***by a solder joint 13 being used to attach a bonding pad of FBAR filter die 12 to signal path 19*** *located within bottom layer 18 of ceramic package 10,* ***and by a solder joint 14 being used to attach another bonding pad of FBAR filter die 12 to signal path 20*** *located within bottom layer 18 of ceramic package 10.*
> (Emphasis added)

Manifestly, contrary to the Examiner's understanding, Bradley shows only a die with two pads, each pad having a single signal path. The use of solder joints to provide the coupling reinforces the physical distinction between the elements. Two separate solder joints makes two separate signal paths 19 and 20, *which are not on the integrated circuit.* Therefore even if one

were to turn to Bradley with the teaching of Lee in mind, there would be no resulting integrated circuit on a single die with two signal paths on the same pad, as claimed in claim 1. The Examiner's understanding of Bradley is simply incorrect!

There is therefore no valid combination of the cited art that leads to the subject matter of claim 1, and the rejection cannot stand.

Each of claims 2-25 is dependent (directly or indirectly) on an allowable independent claim and is likewise allowable without further analysis.

Nonetheless, Applicant notes that the rejection of claims 2-3 and 34-44 (about which more will be said later) is based on a combination of Lee with Bradley and a third reference, Ohnakado. The Examiner indicates that both Lee and Ohnakado "are analogous semiconductor devices having protective circuits" in justifying their combination. He then indicates that the motivation to combine them would have been to obtain "the benefit of forming [a] path for flowing/dispersing large current when a surge due to ESD is impressed from the I/0 pad." However, as further detailed below, this reasoning is specious. Combining Ohnakado's ESD protection with Lee's arrangement may add ESD protection to Lee but it does not yield the claimed invention. If one were to use the motivation posited by the Examiner, one only obtains the Lee arrangement with the ability to shunt an undesired, potentially damaging surge, away from a productive signal-processing path between the dies in a multi-die package. However, the need for surge protection, if present, does not normally relate to the internal connections between the dies in a multi-die package. It exists to protect the external connections so that a surge on external connections should not adversely impact internal components. In other words, the Examiner suggests either an unrealistic combination which would not occur to one skilled in the art or a combination that comes no closer than Lee alone comes to the claimed subject matter.

With respect to claims 26-33, in claim 26 a corresponding amendment is made to that made to claim 1. Thus, claim 26 is limited to an integrated circuit provided on a single die and the above argument applies, *mutatis mutandis*, to this claim. The references do not teach or suggest the subject matter of claim 26, which is thus allowable. Furthermore, the claims dependent thereon are also allowable.

Regarding independent claim 34, such claim has been rejected over a combination of Lee, Bradley and Ohnakado, as mentioned above. However, like claims 1 and 26, claim 34 is drawn to "[a] an integrated circuit comprising, on a single die..." a number of elements. In scope, claim 34 is actually closer to claim 1 than is claim 26, and for all the reasons given above, claim 34 is allowable over the prior art of record. Additionally, Applicant repeats that combining Ohnakado with Lee alone or Lee in combination with Bradley does not lead to the claimed invention. Ohnakado is simply exemplary of an ESD (electro-static-discharge) protection device. Such devices do not include signal paths in the way required in the present claims. Rather, they provide signal shunts which are used to disperse any transient signals away from (not to) sensitive circuitry. In this context, a shunt path is not the same as a signal path in that it absorbs or disperses a signal, keeping it away from the normal operative circuitry of the IC. This is in contrast to a signal path (in the context of the present invention) which provides for conduction of a signal between two locations (i.e., from one to the other) so as to allow further processing of that signal. The purpose and intention of the two is different; they are not analogous. The Examiner has already accepted this as a significant difference in his use of the "dispersing" terminology with reference to the description of the operation of Lee on page 5, where he refers to the *benefit of forming path (sic) for flowing/dispersing large current when a surge due to ESD is impressed from the I/O pad.* Therefore while Ohnakado may describe a MOS device within the circuitry, it is not for the purpose of providing a signal path as is claimed in the present invention. To this end, the Examiner will note that in his reasoning for noting allowability of the subject matter of claim 9, he acknowledges the provision of an impedance device in the second signal path is not taught by the prior art. In the signal shunts of Ohnakado, it would not be possible to provide an impedance device as there would be no dispersion of the signal to ground. In other words, a shunt path is not a signal path.

With respect to the other cited art, as its relevance rests on a valid initial combination of Lee and Bradley, and as this combination can be seen in the light of the above to not be relevant, no comment is required on the other references other than to note that they do not fill the gaps in the prior art teachings noted above.

With regard to claims 4-6, 8, 15-17, 19, 20-21, 27, and 28, it would appear rather far fetched that a person ordinarily skilled in the art would arbitrarily turn to the teachings of **FOUR** or **FIVE** different documents and combine their teachings to arrive at the claimed invention (even if hindsight were to reveal that collectively they disclose all claim limitations, which they do not). The selection of an appropriate four or five would be difficult in itself, but even making a hindsight selection, the Examiner has failed to provide a combination that reads onto the limitations of the independent claims. In this way they also fail to read onto the dependent claims. Moreover, the case law established by the U.S. Court of Appeals for the Federal Circuit (CAFC) requires that the Office establish that any proposed combination of references have been disclosed, suggested or motivated in the prior art, or otherwise be such as would have occurred to one skilled in the art, without use of hindsight. The Examiner's postulated motivations are clearly no more than hindsight justifications for a Monday-morning quarterbacking approach to an obviousness finding - an approach specifically condensed by the CAFC.

For at least these reasons, the rejections should be withdrawn.

CONCLUSION

Applicant has attempted to simplify further reconsideration by avoiding a paragraph-by-paragraph refutation of the Office Action's rejections, and instead discussing primarily the independent claims. Should the Examiner not be convinced that a Notice of Allowance is warranted, however, Applicant wishes the record to be clear that Applicant does not acquiesce in the rejection of any claim and Applicant reserves the right to further prosecute any and all claims.

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance, so that an interview can be arranged.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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